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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 08/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,785	KER ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 - 23* is/are allowed.

6)☒ Claim(s) *1, 2, 4 - 8* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on June 04, 2004. Claim 18 is amended. Amendment and arguments have overcome rejections under 112, 2nd paragraph, objection to the Drawings and some rejections under 103 (a). The rejection follows.

Objection

Claim 23 is objected due to an apparent typing error. The Claim recites: "the functional compartment", while preceding Claim 1 recites: " a functional component". For purpose of examination, the phrase was interpreted as "the functional component".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4 - 6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Puar (US 5,287,241). Puar discloses all the elements of Claims 1 including electrostatic discharge (ESD) protection circuit for an integrated circuit (IC), the ESD protection circuit including: an ESD clamp device (elements D3 and D4 in Fig.4), coupled to a pad (element T2 in Fig.4) and a substrate having a first conductivity type (see Fig. 5, col. 7,

lines 24-57), the ESD clamp device being closed under normal power operation; and a functional component (elements N2, P2 in Fig. 4 and 5), formed on the substrate and coupled to the pad, the functional component having a first well of the first conductivity type (p-type drain well in Fig. 5) and an isolating region of a second conductivity type N-type well in Fig.5), the second conductivity type being the reversed polarity of the first conductivity type, and the isolating region isolating the first well from the substrate; the functional component transmitting signals between the IC and an external linkage under normal power operation.

Regarding Claim 4, Puar discloses the functional component including a metal-oxide semiconductor (MOS) (element N2 in Fig. 4) having the second conductivity type in the first well (see Fig. 5).

Regarding Claim 5, Puar discloses the ESD clamp device including an MOS diode (elements D3 and D4 in Fig. 4) having two ends respectively coupled to the pad and the substrate (see Fig. 5).

Regarding Claim 6, Puar discloses a two-stage ESD protection circuit having a primary ESD protection circuit (element D1 and D2 in Fig. 4) coupled between the pad and the substrate, a secondary ESD protection circuit coupled between the functional component (elements D3 and D4 in Fig. 4) and the substrate, and a resistor (element R2 in Fig. 4) coupled between the functional component and the pad (element T2 in Fig. 4). As to connection to the substrate, Puar discloses that the Vss line of the supply is connected to the substrate (col. 1, lines 41 –57).

Regarding Claim 8, Puar discloses the first conductivity type as an N type, and the second conductivity type as p type (see Fig. 5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Puar in a view of Poplevine et al. (US 6,184,557). As was stated above, Puar discloses all the elements of Claim 1. However, regarding Claim 2, it does not disclose the isolating region having a second well surrounding the first well and a deep well under the first well. Poplevine et al. disclose the functional element structure with the isolating region having a second well (elements 424 and 426 in Fig. 4) surrounding the first well and a deep well under the first well (element 516 in Fig. 4, col. 4, lines 36 – col. 5, line 65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Puar solution by adding the second well and the deep well according to Poplevine et al., because as Poplevine et al. state (col. 3, lines 27 – 34), such a structure would provide more balanced capacitances and resistances and therefore, more symmetric outputs.

Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Puar in a view of Watt (US 5,477,413). As was stated above, Puar discloses all the elements of Claim 1. However, regarding Claim 7, it does not disclose the first conductivity type as an N type, and the second conductivity type as p type. Watt discloses an electrostatic discharge (ESD) protection circuit having the first conductivity type as an N type, and the second conductivity type as p type (see Fig. 5). Both patents have the same problem solving area, namely providing the ESD protection circuit in integrated circuit form. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Puar solution by changing the type of material conductivity from "P" to "N" and vice versa, according to Watt, because as Watt states (col. 9, lines 24 – 34), that his invention can be implemented by a triple well processing (which is usually) a p-well placed into an n-well which itself is in a p-substrate. Thus he suggests that the two technologies are interchangeable. Selection of particular technology is up to the designer.

Allowable Subject Matter

1. Claims 3, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is that Claims 3 and 19 recite the isolating region is coupled to a first power supply and the first well is

coupled to a second power supply. This feature was not founding the collected prior art of the record.

1. Claims 15 - 17 are allowed. A reason for that is that Claim 18 recites, inter alia, an NMOS component formed on a p-type first isolated well on the substrate, an N-type isolating region being formed to separate the p-type first isolated well and the substrate. The collected prior art of the record neither individually, no combined, disclose such combination of limitations.

2. Claims 18 – 23 are allowed. A reason for that is that Claim 18 includes, inter alia, a limitation of a first NMOS component formed on a p-type first isolated well having an N-type isolating region and the NMOS component having the gate connected to the high power line. The collected prior art of the record neither individually, no combined, disclose such combination of limitations.

3. Claims 9 – 14 are allowed. A reason for that is that Claim 9, inter alia, discloses an NMOS component formed in the first well on the substrate having a first conductivity type and an isolating region having the second conductivity type. The collected prior art of the record neither individually, no combined, disclose such combination of limitations.

Response to Arguments

Applicant's arguments filed June 04, 2004 have been fully considered. Some of the arguments were taken into account resulting in newly allowed claims. However, following arguments are not persuasive.

1. Regarding Claim 1 rejection, the Applicant alleges that the p-type doped region in Fig. 5 of Puar is the drain of the PMOS transistor and therefore "one of ordinary skill in the art would not read a drain region of a MOS as a well region due to different doped concentrations". However, according to the R. Graf, Modern Dictionary of Electronics, the well is defined as "a region of silicon formed by introducing impurities of opposite polarity, usually in the substrate; used to separate MOS transistors there". As well known in the art, the doped concentrations can have wide range of variations. The particular doped concentrations of impurities neither stated in the claim, nor in the Specification.

The same argument is recited again regarding the Claim 2, 4 and 7rejections.

2. As to rejection of Claim 2, the Applicant further states that he had different reason for introducing the isolating well than the reference (page 13, lines 4 – 12), i.e. the recited structure was intended for different use. This issue was addressed by the Court stating that "it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham,* 2 USPQ2d 1647 (1987).

Finally, the Applicant alleges: "one of ordinary skill in the art would have no motivation to combine Puar and Poplevine et al. to obtain the claimed invention" without giving any supporting evidence for such statement. The Claim 2 rejection includes an appropriately formulated motivation.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.

08/10/2004

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